Amendment in the Claims

Claims 1-57 (cancelled).

58. (Currently Amended) ~~The processor of claim 57~~A processor, comprising a Boolean logic unit, wherein the Boolean logic unit is operable for performing the short-circuit evaluation of Normal Form Boolean expressions/operations; a plurality of input/output interfaces, wherein the plurality of input/output interfaces are operable for receiving a plurality of compiled Boolean expressions/operations and transmitting a plurality of compiled results; and a plurality of multi-bit registers, wherein the plurality of multi-bit registers comprise an instruction register, a first address register and a second address register, wherein if the Boolean logic unit is operable for performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations, then the first address register is a next operation address register and the second address register is an end of OR address register, wherein if the Boolean logic unit is operable for performing the short-circuit evaluation of Disjunctive Normal Form Boolean expressions/operations, then the first address register is an end of operation address register and the second address register is an end of AND address register, and if the Boolean logic unit is operable for performing the short-circuit evaluation of both Conjunctive and Disjunctive Normal Form Boolean expressions/operations, then the first address register is a next operation/end of operation address register and the second address register is an end of OR/AND address register.

59. (Original) The processor of claim 58, wherein the instruction register comprises a register that is n+m+x bits wide and includes an n-bit address, an m-bit control/state word, and an x-bit operational code.

60. (Original) The processor of claim 59, wherein the instruction register comprises a register that is n+m+3 bits wide and includes an operational code that is 3 bits wide.

61. (Original) The processor of claim 59, wherein the operational code is more than 3 bits wide.

62. (Original) The processor of claim 59, wherein the first and second address registers are n+m

bits wide, and wherein the Boolean logic unit is operable to load both the n-bit address and the m-bit wide control/state word from the instruction register into the first and second address registers to form an address that is n+m bits wide.

63. (Original) The processor of claim 59, wherein the Boolean logic unit is operable to associate each of a plurality of logical addresses with a respective physical address in a control store, and operable to retrieve a particular physical address from the control store based on the associated logical address present in one of the first or second address registers.

64. (Original) The processor of claim 58, wherein the first address register stores an address used for Boolean short-circuiting.

65. (Original) The processor of claim 58, wherein the second address register stores the address of an instruction immediately following a conjunct comprising an OR clause, or the address of an instruction immediately following a disjunct comprising an AND clause.

Claims 66-102 (cancelled).

103. (Currently Amended) ~~The computing device of claim 102,~~ A computing device, comprising: a general-purpose processor; and a Boolean co-processor that accepts code, representative of Boolean code, from the general-purpose processor, the Boolean processor including:

a Boolean logic unit, wherein the Boolean logic unit is operable for performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations, operable for performing the short-circuit evaluation of Disjunctive Normal Form Boolean expressions/operations, or operable for performing the short-circuit evaluation of both Conjunctive Normal Form Boolean expressions/operations and Disjunctive Normal Form Boolean expressions/operations;

a plurality of input/output interfaces, wherein the plurality of input/output interfaces are operable for receiving a plurality of compiled Boolean expressions/operations and transmitting a plurality of compiled results; and

a plurality of multi-bit registers, wherein the plurality of multi-bit registers comprise an instruction register, a first address register and a second address register, wherein if the Boolean logic unit is operable for performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations, then the first address register is a next operation address register and the second address register is an end of OR address register, wherein if the Boolean logic unit is operable for performing the short-circuit evaluation of Disjunctive Normal Form Boolean expressions/operations, then the first address register is an end of operation address register and the second address register is an end of AND address register, and if the Boolean logic unit is operable for performing the short-circuit evaluation of both Conjunctive and Disjunctive Normal Form Boolean expressions/operations, then the first address register is a next operation/end of operation address register and the second address register is an end of OR/AND address register.

104. (Original) The computing device of claim 103, wherein the instruction register comprises a register that is n+m+x bits wide and includes an n-bit address, an m-bit control/state word, and an x-bit operational code.

105. (Original)The computing device of claim 103, wherein the first address register stores an address used for Boolean short-circuiting.

106. (Original) The computing device of claim 103, wherein when evaluating Conjunctive Normal Form Boolean expressions/operations, the second address register stores the address of an instruction immediately following a conjunct comprising an OR clause, and when evaluating Disjunctive Normal Form Boolean expressions/operations, the second address register stores the address of an instruction immediately following a disjunct comprising an AND clause.

107. (Original) The computing device of claim 106, wherein the instruction whose address is stored in the second address register is another conjunct or disjunct, respectively.

Claims 108-126 (cancelled).

127. (Currently Amended) ~~The hybrid processor of claim 126~~ A hybrid processor, comprising: a host processor, wherein the host processor is at least operable for performing comparison operations and register modifications; and a Boolean processor core, comprising:

a Boolean short-circuit outcome calculation unit, wherein the Boolean short-circuit outcome calculation unit is operable for evaluating the short-circuit outcome of Conjunctive Normal Form Boolean expressions/operations, operable for evaluating the short-circuit outcome of Disjunctive Normal Form Boolean expressions/operations, or operable for evaluating the short-circuit outcome of both Conjunctive Normal Form Boolean expressions/operations and Disjunctive Normal Form Boolean expressions/operations;

a plurality of input/output interfaces, wherein the plurality of input/output interfaces are operable for receiving, from the host processor, data related to a plurality of compiled Boolean expressions/operations and transmitting, to the host processor, data representative of the short-circuit outcome of a plurality of evaluated Normal Form Boolean expressions/operations; and

a plurality of multi-bit registers., wherein the plurality of multi-bit registers comprise a first address register and a second address register, wherein if the Boolean short-circuit outcome calculation unit is operable for evaluating the short-circuit outcome of Conjunctive Normal Form Boolean expressions/operations, then the first address register is a next operation address register and the second address register is an end of OR address register, wherein if the Boolean short-circuit outcome calculation unit is operable for evaluating the short-circuit outcome of Disjunctive Normal Form Boolean expressions/operations, then the first address register is an end of operation address register and the second address register is an end of AND address register, and if the Boolean short-circuit outcome calculation unit is operable for evaluating the short-circuit outcome of both Conjunctive and Disjunctive Normal Form Boolean expressions/operations, then the first address register is a next operation/end of operation address register and the second address register is an end of OR/AND address register.

128. (Original) The hybrid processor of claim 127, wherein the first register stores an

address used by the host processor for Boolean short-circuiting.

129. (Original) The hybrid processor of claim 127, wherein when evaluating Conjunctive Normal Form Boolean expressions/operations, the second address register stores the address of an instruction immediately following a conjunct comprising an OR clause, and when evaluating Disjunctive Normal Form Boolean expressions/operations, the second address register stores the address of an instruction immediately following a disjunct comprising an AND clause.

130. (Original) The hybrid processor of claim 127, wherein at least one of the first and second address registers stores an address that is transmitted to the host processor by the plurality of input/output interfaces as the short-circuit outcome of a plurality of evaluated Normal Form Boolean expressions/operations.

131. (Original) The hybrid processor of claim 130, wherein the address is transmitted to a memory device in the host processor.

132. (Original) The hybrid processor of claim 131, wherein the address is transmitted to a register in the host processor.

133. (Original) The hybrid processor of claim 131, wherein the address is transmitted to a program counter in the host processor.

134. (Original) The hybrid processor of claim 127, wherein loading the first address register activates the Boolean processor core.

135. (Original) The hybrid processor of claim 127, wherein a predetermined input from the host processor deactivates the Boolean processor core, thereby preventing the Boolean processor core from transmitting, to the host processor, any short-circuit outcome data.

136. (Original) The hybrid processor of claim 127, wherein a predetermined input from

the host processor resets an OR conjunct and/or AND disjunct register, thereby notifying the Boolean processor core than an OR conjunct or AND disjunct has ended.

Claims 137-146 (cancelled).